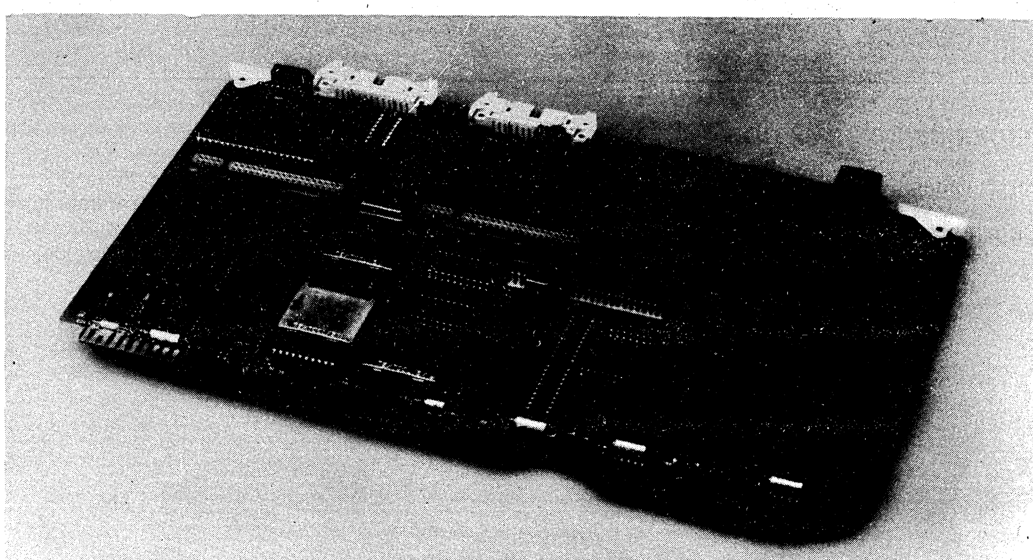
PRELIMINARY

iSBC® 186/51 COMMUNICATING COMPUTER

- 8 MHz iAPX 186 Microprocessor
- 128K Bytes of dual-ported RAM expandable on-board to 256K Bytes
- 82586 Local Communications Controller for CSMA/CD applications and 82501 Ethernet serial interface for Ethernet/ IEEE 802 specifications
- Two serial interfaces, RS-232C and RS-422A/RS-449 compatible
- Sockets for up to 192K Bytes of JEDEC 28 pin standard memory devices
- 80130 Real-Time Operating System Firmware
- Two iSBX™ bus connectors
- 16M Bytes address range of MULTIBUS®
- MULTIBUS® interface for multimaster configurations and system expansion
- Supported by a complete family of single board computers, peripheral controllers, digital & analog I/O, memory, packaging and software

The iSBC® 186/51 COMMUNICATING COMPUTER is a member of Intel's large COMMputer™ family of microcomputer products that utilizes Intel's VLSI technology to provide an economical self-contained computer for applications in data communications and local area network control. The combination of the iAPX 186 Central Processing Unit/80130 Operating System Firmware and the 82586 Local Communications Controller/82501 Ethernet Serial Interface makes it ideal for applications which require both communication and processing capabilities such as networked workstations, factory automation, office automation, communications servers, and many others. The CPU, Ethernet interface, serial communications interface, 128K Bytes of RAM, up to 192K Bytes of ROM, Operating System Firmware, I/O ports and drivers and the MULTIBUS® interface all reside on a single 6.75" × 12.00" printed circuit board.



JULY 1983
ORDER NUMBER: 230718-001

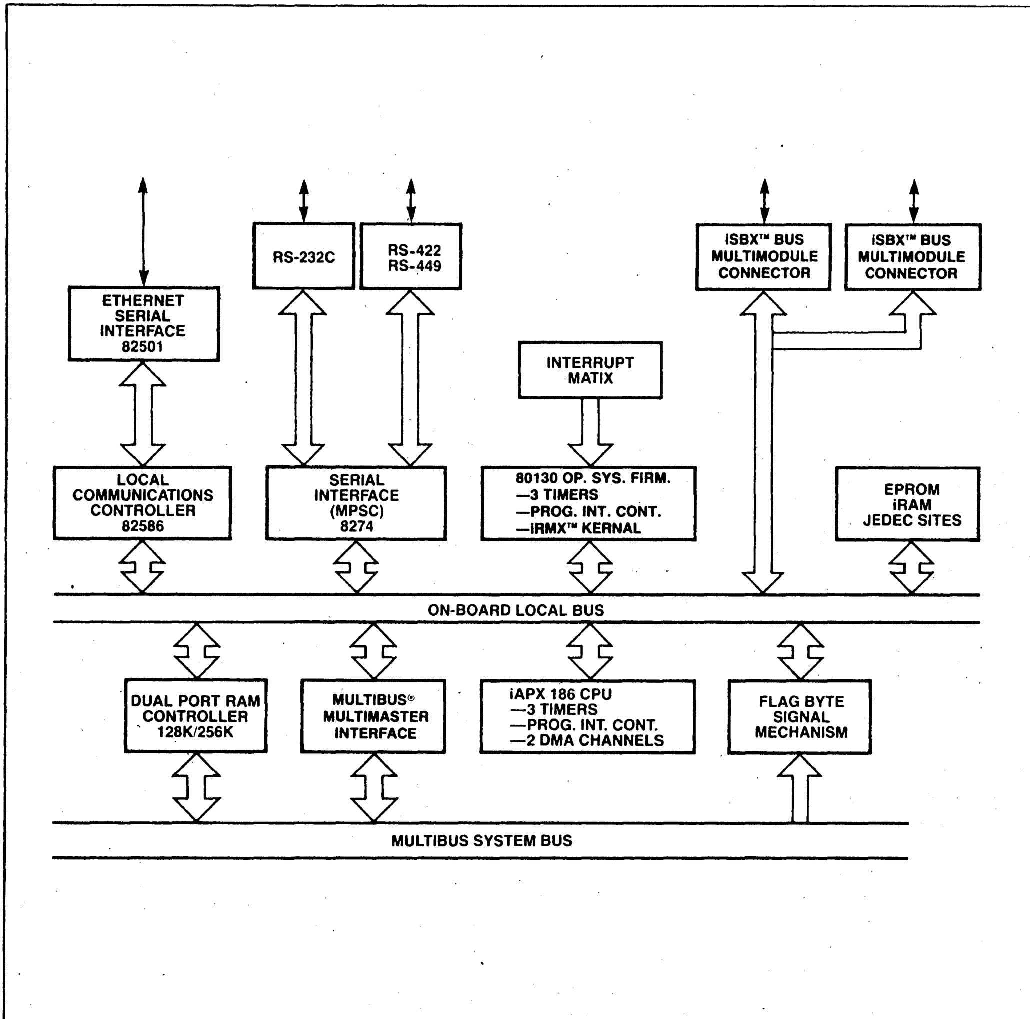


Figure 1. iSBC® 186/51 Block Diagram

FUNCTIONAL DESCRIPTION

Communicating Computer

The iSBC® 186/51 board integrates a programmable processor and communications capability onto one board, serving both computational and networking capacities as dictated by the application. The communications co-processor (82586) aids in this task by accomplishing as much of the communications task as possible before the processor intervenes (thus reducing the overhead load of the 80186 processor).

The integration of the communication and processing capabilities onto one board results in two primary benefits: (1) increased performance with elimination of system bus arbitration and (2) increased savings due to the compact, one-board design.

The dual capabilities of the iSBC 186/51 are useful in three types of applications: (1)as a single board communicating computer running both user applications and communications tasks; (2)as one bus master of a multiple processor board solution running a portion of the overall user application and the communications tasks; and (3) as an "intelligent bus slave" that performs communications related tasks as a peripheral processor to one or more bus masters in a communications intensive environment.

Architecture

The iSBC 186/51 board is functionally partitioned into three major sections: central computer, I/O including LAN interconnect and memory including shared dual port RAM (Figure 1).

The central computer, with an iAPX 186 CPU and the 80130 Operating System Firmware (OSF) provides powerful processing capability. The microprocessor and OSF primitives, together with the on-board PROM/EPROM sites, programmable timers/counters, and programmable interrupt control provide the intelligence to manage sophisticated communications operations on-board the iSBC 186/51. The timers/counters and interrupt control are also common to the I/O area providing programmable baud rates to the USARTs and prioritizing interrupts generated from the USARTs. The central computer functions are protected for access by the on-board 80186 only.

The I/O is centered around the Ethernet access provided by the 82586/82501 pair. All CSMA/CD protocols can be supported. Included here as well are two serial interfaces, both of which are fully programmable. In support of the single board computer, two iSBX connectors are provided for further customer expansion of I/O capabilities. The I/O is under full control of the on-board CPU and is protected from access by other system bus masters.

The third major segment, dual-port RAM memory, is the key link between the 80186, the Ethernet controller, and bus masters (if any) managing the system functions. The dual-port concept allows a common block of dynamic memory to be accessed by the on-board 80186 CPU, the on-board Ethernet controller and off-board bus masters. The system program can, therefore, utilize the shared dual-port RAM to pass command and status information between the bus masters and on-board CPU and Ethernet controllers. In addition, the dual-port concept permits blocks of data transmitted or received to accummulate in the on-board shared RAM, minimizing the need for a dedicated memory board.

CENTRAL COMPUTER FUNCTIONALITY

Central Processing Unit

The central processor for the iSBC 186/51 is Intel's iAPX 186 CPU. The iAPX 186 is a high integration 16-bit microprocessor. It combines several of the most common system components onto the chip (i.e., Direct Memory Access, Interval Timers, Clock generator, and Programmable Interrupt Controller) and provides a performance improvement of 30% over the 8086-2 processor. The CPU architecture includes four 16-bit Byte addressable data registers, two 16-bit index registers and two 16-bit memory base pointer registers. These are accessible by a total of 24 operand addressing modes for (1) comprehensive memory addressing, and (2) support of the data structures required for today's structured, high level languages—as well as assembly language.

Instruction Set

The iAPX 186 instruction set is a superset of the 8086. It maintains object code compatibility while adding 10 new instructions to the existing iAPX 86 instruction set. The iAPX 186 retains the variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulations. Added instructions include: Block I/O, Enter and Leave subroutines, Push Immediate, Multiply Quick, Array Bounds Checking, Shift and Rotate by Immediate, and Pop and Push All.

Architectural Features

A six-byte instruction queue provides prefetching of sequential instructions and can reduce the 750 nsec minimum instruction cycle to 250 nsec for queued instructions. The stack oriented architecture readily supports modular programming by facilitating fast, simple, intermodule communication, and other programming constructs needed for asynchronous real-time systems. Using a windowing technique and external logic, the full 16M Bytes addressing range of the IEEE-796 MULTIBUS Standard is available to the user. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K Bytes at a time and activation of a specific register is controlled, both explicitly by program control, and implicitly by specific functions and instructions. A flag byte signaling mechanism aids in creating an interprocessor communication scheme. This includes (1) the ability to set/reset interrupts with MULTIBUS commands and (2) board reset.

OPERATING SYSTEM FUNCTIONALITY

Operating System Firmware

The 80130 provides a set of multitasking kernel primitives, kernel control storage, and the additional support hardware, including system timers and interrupt controller, required by those primitives. To the applications programmer, the OSF extends the iAPX 186 architecture by providing 35 operating system primitive instructions, and supporting five new system data types. This makes the OSF a logical and easy to use architectural extension to the iAPX 186 system design. The chip has also been designed to be compatible with the iRMX86 operating system.

Architecture

The 80130 is connected directly to the local bus of the 80186 processor with address decoding, buffering, and bus-demultiplexing logic contained on-chip (Figure 1). Internally, the 80130 firmware consists of two sections: an operating system unit and a control unit. The former consists of a 16K Byte operating-system-kernel control store complete with an operating-system timer, a delay timer, a bit-rate generator, and 8259A-compatible programmable interrupt logic.

The first timer generates the fundamental real-time clock period in the system. It is set to 10 milliseconds initially but can be modified by the system designer. The delay timer supports the kernel timing function by indicating the next event. Both these timer resources are reserved for use by the kernel.

The bit-rate generator, which has a range of 75 to 768 kilobits per second, is provided as a user resource. The 80130 interrupt logic vectors eight independent priority levels, one of which is reserved for the operating-system timers.

Operation

The 80130 supplements the 80186's basic architecture with five new objects, or system data types: jobs, tasks, segments, mailboxes, and regions. See Tables 1 and 2 for the new data types and operating system primitives.

The 80130 operates by creating, manipulating and deleting individual system objects. When an object is created, the 80130 returns its name to the creating task. This name is referred to and used as an abstract data type, called a TOKEN. The TOKEN is a highly efficient way of accessing the iSBC 186/51 address space. Referring to a segment object, for example, causes a 16-bit address to be loaded into one of the processor segment registers, which can then be used to directly address a paragraph (16-Byte unit) anywhere in the 1M Byte address space. Task creation is also accomplished in this manner and requires only the specification of a priority, a task private data segment (if needed), a task stack, and a task program starting address.

To take full advantage of multiprogramming, the operating system must provide each application with a separate environment—that is, separate memory and tasks. This isolation both protects independent programs from interfering with one another and allows the application programmer to work without regard to the other application programs in the system. The 80130 supports multiprogramming with the job data type. The creation of a job requires the specification of a large number of parameters and is normally done only when the system is being initialized.

Table 1. System Data Types Used in 80130 Operating System Firmware

Job	Jobs are the means of organizing the program environment and resources. An application consists of one or more jobs. Each iAPX 186 system data type is contained in some job. Jobs are independent of each other, but they may share access to resources. Each job has one or more tasks, one of which is an initial task. Jobs are given pools of memory, and they may create subordinate offspring jobs, which may borrow memory from their parents.
Task	Tasks are the means by which computations are accomplished. A task is an instruction stream with its own execution stack and private data. Each task is part of a job and is restricted to the resources provided by its job. Tasks may perform general interrupt handling as well as other computational functions. Each task has a set of attributes, maintained for it by the iAPX 186, which characterize its status. These attributes are: its containing job its register context its priority (0-255) its execution state (asleep, suspended, ready, running, asleep/suspended) its suspension depth its user-selected exception handler its option 8087 extended task state
Segment	Segments are the units of memory allocation. A segment is a physically contiguous sequence of 16-Byte, 8086 paragraph-length, units. Segments are created dynamically from the free memory space of a Job as one of its Tasks requests memory for its use. A segment is deleted when it is no longer needed. The iAPX 186 maintains and manages free memory in an orderly fashion, it obtains memory space from the pool assigned to the containing job of the requesting task and returns the space to the job memory pool (or the parent job pool) when it is no longer needed. It does not allocate memory to create a segment if sufficient free memory is not available to it; in that case it returns an error exception code.
Mailbox	Mailboxes are the means for intertask communication. Mailboxes are used by tasks to send and receive message segments. The iAPX 186 creates and manages two queues for each mailbox. One of these queues contains message segments sent to the mailbox but not yet received by any task. The other mailbox queue consists of tasks that are waiting to receive messages. The iAPX 186 assures that waiting tasks receive messages as soon as messages are available. Thus at any moment one or possibly both of two mailbox queues will be empty.
Region	Regions are the means of serialization and mutual exclusion. Regions are familiar as "critical code regions." The iAPX 186 region data type consists of a queue of tasks. Each task waits to execute in mutually exclusive code or to access a shared data region, for example to update a file record.
Tokens	The OSP interface makes use of a 16-bit TOKEN data type to identify individual OSF data structures. Each of these (each instance) has its own unique TOKEN. When a primitive is called, it is passed the TOKENs of the data structures on which it will operate.

Table 2. 80130 Operating System Firmware Primitives

JOB	CREATE JOB	Creates a job partition including memory pool, task list, and stack area.
TASK	CREATE TASK	Creates a task with the specified environment and priority and puts it in the ready state. Checks for insufficient memory available within the containing job.
	DELETE TASK	Deletes a task from the system as well as from any queues in which it is waiting. The task's state and stack segment are de-allocated.
	SUSPEND TASK	Suspends a task (changes its status to suspended) or increases the task's suspension count by 1. A sleeping task may also be suspended and will then awaken suspended unless resumed.
	RESUME TASK	Decreases the suspension count of a task by 1. If the count is at that point reduced to 0, the task state is made ready or if it was suspend-asleep, it is put back to asleep.
	SLEEP	Puts the task in the asleep state, a number of 10-ms units may be specified.
INTERRUPT	SET PRIORITY	Changes the task's priority to the value passed in the primitive.
	SET INTERRUPT	Assigns an interrupt handler to a level. The task that makes this call is made the interrupt task for the same level, unless the call indicates there is no interrupt task.
	RESET INTERRUPT	Disables an interrupt level. Cancels the interrupt handler, deletes the interrupt task for that level if assigned.
	GET LEVEL	Returns the number of the interrupt level for highest priority interrupt handler currently in operation (several interrupt handlers could be operating).
	EXIT INTERRUPT	Completes interrupt processing and sends end-of-interrupt signal to hardware.
	SIGNAL INTERRUPT	Invokes the interrupt task assigned to a level from that level's interrupt handler.
	WAIT INTERRUPT	Makes the interrupt task state suspended pending a signal interrupt from an interrupt handler. Used by an interrupt task to signal its readiness to service an interrupt.
	ENABLE	Enables an external interrupt level.
	DISABLE	Disables an external interrupt level.
	GET EXCEPTION HANDLER	Reads the location and exception-handling mode of the current operating system exception handler for a task.
	SET EXCEPTION HANDLER	Establishes the location and exception-handling mode of the current operating system exception handler for a task.

Table 2. 80130 Operating System Firmware Primitives (Cont.)

SEGMENT	CREATE SEGMENT	Allocates dynamically an area of memory of a specified length in 16-Byte paragraph units up to a maximum of 64K Bytes (for example, for use as a buffer). Returns a location token for the segment allocated.
	DELETE SEGMENT	De-allocates the memory segment indicated by the parameter token.
	ENABLE DELETION	Allows the system data type value indicated by the location token to be deleted.
	DISABLE DELETION	Prevents the system data type value indicated by the location token from being deleted.
MAILBOX	CREATE MAILBOX	Creates a mailbox with the specified task queueing discipline. Returns a location token.
	DELETE MAILBOX	Deletes a mailbox, and returns its memory. If tasks are waiting for the mailbox, they are awakened (their state is made ready) with an appropriate exception condition. If messages are waiting for tasks, they are discarded.
	SEND MESSAGE	Sends a message segment to a mailbox.
	RECEIVE MESSAGE	A task is ready to receive a message at a mailbox. The task is placed on the mailbox task queue. The task may optionally wait for a response indefinitely, or a number of time intervals (generally 10 ms long), or not at all. When complete, the primitive returns to the task the location token of the message segment received.
REGION	CREATE REGION	Creates a region data type value specifying a queueing discipline. Returns a token for the region.
	DELETE REGION	Deletes a region if and only if the region is not in use.
	ACCEPT CONTROL	Gains control of a region if it is immediately available, but does not wait if it is not available.
	RECEIVE CONTROL	Is the same primitive as accept control but the task that performs it may elect to wait.
	SEND CONTROL	Relinquishes a region.

Programmable Timers

The 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (two per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source. The factory default configuration for timer 0 is baud rate generator.

The 80130 provides three more programmable timers. One is a factory default baud rate generator and outputs an 8254 compatible square wave to the RS232 Channel B. The other two timers are assigned to the use of the OSF and should not be altered by the user.

The system software configures each timer independently to select the desired function. Examples of available functions are shown in Table 3. The contents of each counter may be read at any time during system operation.

Interrupt Capability

The iSBC 186/51 has two programmable interrupt controllers (PICs): one in the 80186 component and one in the 80130 component. In the iRMX mode, the 80186 interrupt controller acts as a slave to the 80130. The 80186 interrupt controller in this mode uses all of its external interrupt pins. It therefore services only internally generated interrupts (i.e., three timers, two DMA channels). The 80130 interrupt controller operates in the master mode and has eight prioritized inputs that can be programmed either edge or level sensitive.

The iSBC 186/51 board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 80186 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Programmable Interrupt Controllers (PIC) provide control and vectoring for the next eight interrupt levels. As shown in Table 4, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating modes and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU.

Interrupt Request Generation

iSBC 186/51 Interrupt Service requests may originate from 25 sources. Table 5 contains a list of devices and functions supported by interrupts. All interrupts are jumper configurable with either suitcase or wire wrap to the desired interrupt request level.

Table 3. 80186 Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until 1/2 the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N periods after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 4. iSBC® 186/51 Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Special fully nested	Allows multiple interrupts from slave PICs to the master PIC. Used in the case of cascading where the priority has to be conserved within each slave.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Table 5. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS® interface	Requests from MULTIBUS® resident peripherals or other CPU	2
8274	Transmit buffer empty, receive buffer full and channel errors	8
Internal 80186 PIC	Timer 0, 1, 2 outputs (function determined by timer mode) and 2 DMA channel interrupts	5
82586 LCC	Communications processor needs attention	1
Flag byte interrupt	Flag byte interrupt set by MULTIBUS master	1
Systick	80130, MRX system timer	1
Edge to level trigger	Converts EDGE interrupts to level interrupts	1
iSBX™ connectors MULTIMODULE™	Function determined by iSBX™	4 (2 per iSBX connector)
Bus fail safe timer	Indicates addressed MULTIBUS® resident device has not responded to command within 6 msec	1
OR-gate matrix	Outputs of OR-gates on-board for multiple interrupts	1

I/O FUNCTIONALITY

Local Communications Controller

The 82586 is a local communications controller designed to relieve the iAPX 186 of many of the tasks associated with controlling a local network. The 82586 provides most of the functions normally associated with the data link and physical link layers of a local network architecture. In particular, it performs framing (frame boundary delineation, addressing, and bit error detection), link management, and data modulation. It also supports a network management interface.

The iAPX 186 and the 82586 communicate entirely through a shared memory space. To the user, the 82586 appears as two independent but communicating units: the Command Unit (CU) and the Receive Unit (RU). The CU executes the commands given by

the iAPX 186 to the 82586. The RU handles all activities related to packet reception, address recognition, CRC checking, etc. The two are controlled and monitored by the CPU via a shared memory structure called the System Control Block (SCB). Commands for the CU and RU are placed into the SCB by the host processor. Status information is placed into the SCB by the CU and RU (via the CU). The Channel Attention and Interrupt lines are used by the CU and the 82586 to get the other to look into the SCB. See Figure 2.

The 82586 features a high level diagnostic or maintenance capability. It automatically gathers statistics on CRC errors, frame alignment errors, overrun errors, and frames lost due to lack of reception resources. In addition, the user can output the status of all internal registers to facilitate system design.

Upon initialization, the 82586 obtains the address of its System Control Block through the Initialization Root which begins at location 0FFFFF6H. See Figure

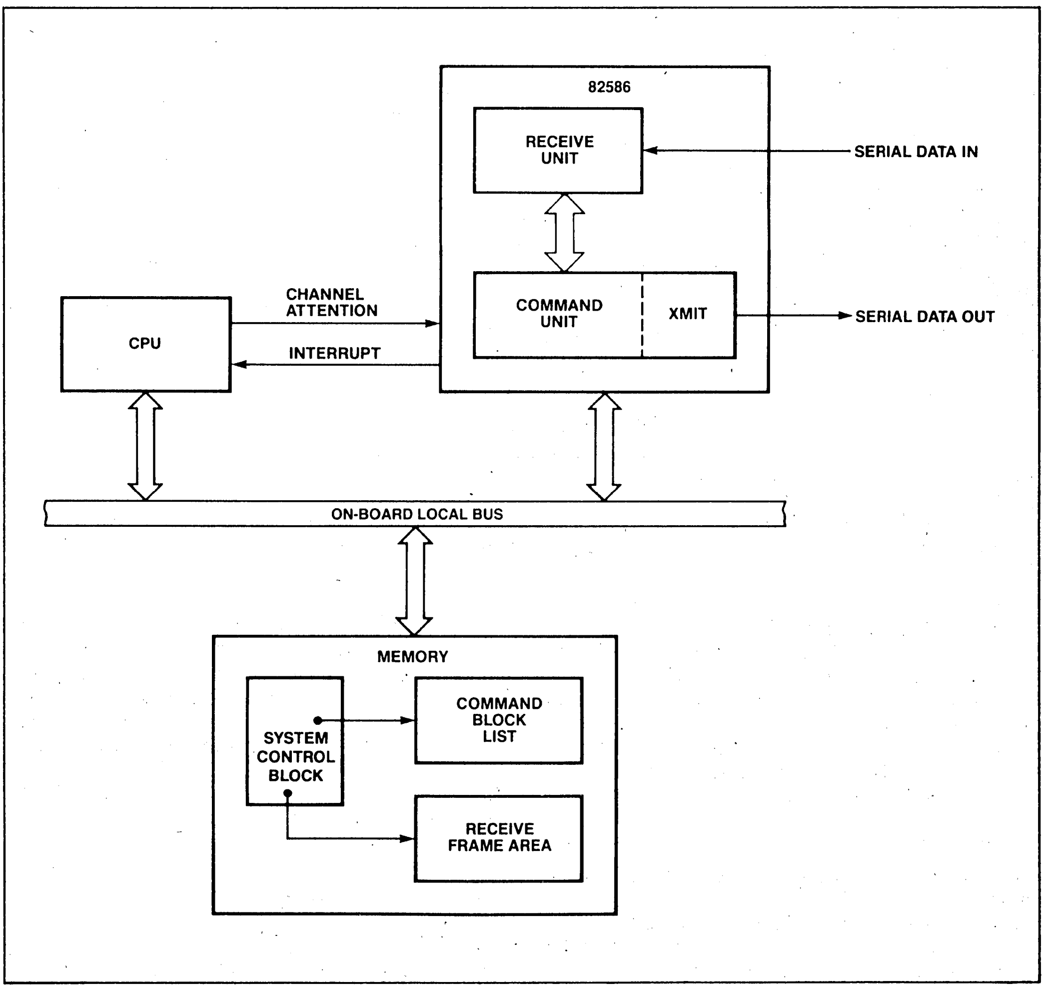


Figure 2. System Overview

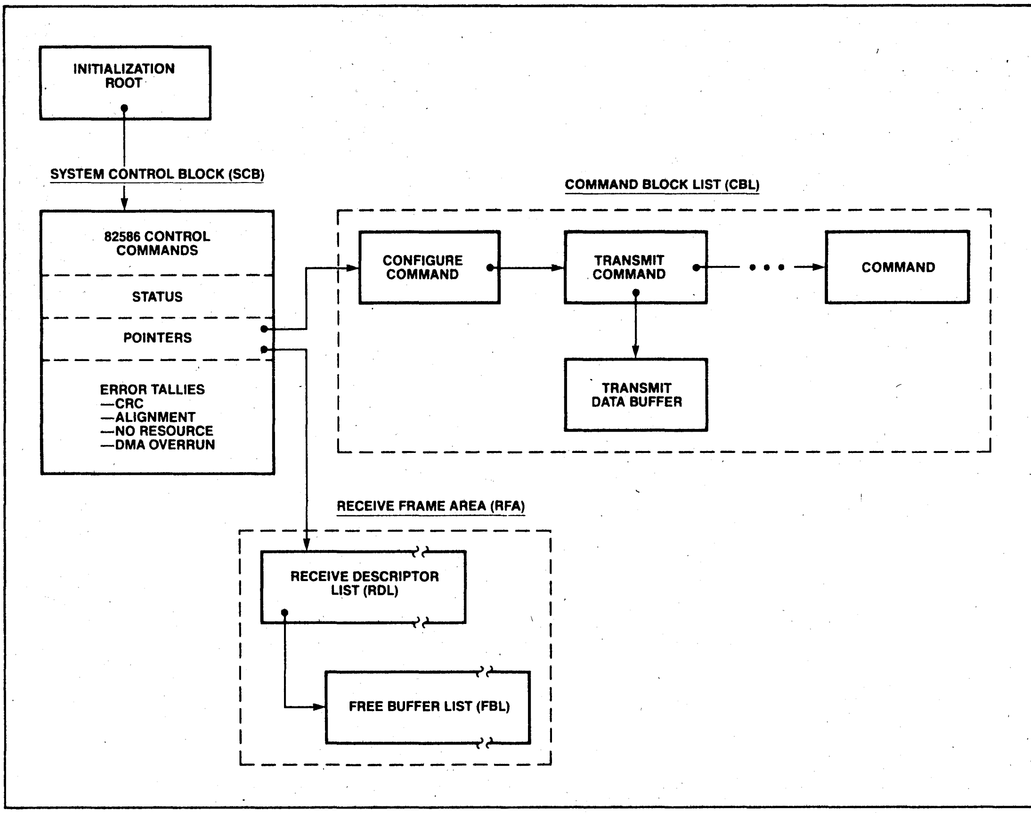


Figure 3. 82586 Memory Structures

3. The SCB contains control commands, status register, pointers to the Command Block List (CBL) and Receive Frame Area (RFA), and tallies for CRC, Alignment, DMA Overrun and No Resource errors. Through the SCB, the 82586 is able to provide status and error counts for the iAPX 86, execute "programs" contained in the CBL and receive incoming frames in the Receive Frame Area (RFA).

Serial I/O

Two programmable communications interfaces using the Intel 8274 Multi-Protocol Serial Controller (MPSC) are contained on the iSBC 186/51. Two independent software selectable BAUD rate generators provide the channels with all the common communications frequencies. The mode of operation (i.e., Asynchronous, Byte Synchronous or Bisynchronous protocols), data format, control character format, parity, and baud rate are all under program control. The 8274 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the MPSC. The iSBC 186/51 supports operation in the polled, interrupt and DMA driven interfaces through jumper options. The board comes factory defaulted with channel A in RS-422A/RS-449, channel B in RS-232C. Channel A can be configured to support RS-232C also.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 186/51 microcomputer. Through these connectors, additional on-board I/O functions

may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost results when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 186/51 boards provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBC MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 186/51 microcomputers. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 186/51 boards. An iSBX bus interface specification and iSBX connectors are available from Intel.

MEMORY FUNCTIONALITY

RAM Capabilities

The iSBC 186/51 COMMputer board contains 128K Bytes of dual-port dynamic RAM. The on-board RAM may be expanded to 256K Bytes with the iSBC 304 MULTIMODULE board mounted onto the iSBC 186/51 board. The dual-port controller allows access to the on-board RAM (including RAM MULTIMODULE options) from the iSBC 186/51 board and from any other MULTIBUS master via the system bus. Segments of on-board RAM may be configured as a private resource, protected from MULTIBUS system access. The amount of memory allocated as a private resource may be configured in increments of 25% of the total on-board memory ranging from 0% to 100% (optional RAM MULTIMODULE board doubles the increment size). These features allow the multiprocessor systems to establish local memory for each processor and shared system memory configurations where the total system memory size (including local on-board memory) can exceed one megabyte without addressing conflicts.

Universal Memory Sites for Local Memory

Six 28-pin sockets are provided for the use of Intel's 2732, 2764, 27128, 27256 EPROMs and their respective ROMs. When using the 27256s, the on-board EPROM capacity is 192K Bytes. Other JEDEC standard pinout devices are also supported, including byte-wide static RAMs and iRAMs.

MULTIBUS® SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus is Intel's industry standard microcomputer bus structure. Both 8 and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPU's and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 186/51 boards provide full MULTIBUS arbitration control logic. This control logic allows up to *three iSBC 186/51 boards* or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme. This allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with

multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

MISCELLANEOUS FUNCTIONALITY

Power-Fail Control and Auxiliary Power

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

System Development Capabilities

The development cycle of iSBC 186/51 products can be significantly reduced and simplified by using either the System 86/3XX or the Intellec Series Microcomputer Development Systems. The Assembler, Locating Linker, Library Manager, Text Editor and System Monitor are all supported by the ISIS-II disk-based operating system. To facilitate conversion of 8080A/8085A assembly language programs to run on the iSBC 186/51 boards, CONV-86 is available under the ISIS-II operating system.

In-Circuit Emulator

The Integrated Instrumentation In-Circuit Emulator (I^2ICE) provides the necessary link between the software development environment provided by the Intellec system and the "target" iSBC 186/51 execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 186/51 boards, the I^2ICE-186 provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

PL/M-86 and C-86

Intel has two systems implementation languages, PL/M-86 and C-86. Both are standard in the System 86/3XX and are also available as Intellec Microcomputer Development System options. PL/M-86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still allowing explicit control of the system's resources when needed. C-86 is especially appropriate in applications requiring portability and code density. FORTRAN 86 and PASCAL 86 are also available on Intellec or 86/3XX systems.

Run-Time Support

Intel also offers two run-time support packages: iRMX 88 Realtime Multitasking Executive and the iRMX 86 Operating System. The iRMX 88 executive is a simple, highly configurable and efficient foundation for small, high performance applications. Its multitasking structure establishes a solid foundation for modular system design and provides task scheduling and management, intertask communication and synchronization, and interrupt servicing for a variety of peripheral devices. Other configurable options include terminal handlers, disk file system, debuggers and other utilities. The iRMX 86 Operating System is a highly functional operating system with a very rich set of features and options based on an object-oriented architecture. In addition to being modular and configurable, functions beyond the nucleus include a sophisticated file management and I/O system, and a powerful human interface. Both packages are easily customized and extended by the user to match unique requirements.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, or 32 bits
Data—8, 16 bits

System Clock

8.00 MHz ± 0.1%

Cycle Time

Basic Instruction Cycle

8 MHz—750 ns
—250 ns (assumes instruction in the queue)

Note: Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles.)

Memory Response Time

	Max Access Time	Min Cycle Time
RAM	—	750ns
Universal Memory Sites	200ns	500ns
(jumper selectable)	300ns	625ns

Memory Capacity/Addressing

Six Universal Memory Sites support JEDEC 24/28 pin EPROM, PROM, iRAM and static RAM.

Example for EPROM:

Device	Total Capacity	Address Range
2732	24K Bytes	$F8000\text{-}FFFFF_H$
2764	48K Bytes	$F0000\text{-}FFFFF_H$
27128	96K Bytes	$E0000\text{-}FFFFF_H$
27256	192K Bytes	$C0000\text{-}FFFFF_H$

On-Board RAM

Board	Total Capacity	Address Range
iSBC 186/51	128K Bytes	$0\text{-}1FFFF_H$

With Multimodule™ RAM

Board	Total Capacity	Address Range
iSBC 304	256K Bytes	$0\text{-}3FFFF_H$

I/O Capacity

Serial—two programmable channels using one 8274
iSBX™ Multimodule™—two 8/16-bit iSBX™ connectors allow use of up to 2 single-wide modules or 1 single-wide module and 1 double-wide iSBX module.

Serial Communications Characteristics

Synchronous —5-8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous —5-8 bit characters; break character generation; 1, 1/2, or 2 stop bits; false start bit detection

Baud Rates

Frequency (KHz) (S/W Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
	÷1	÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38,400	2400	600
19.2	19,200	1200	300
9.6	9,600	600	150
4.8	4,800	300	75
2.4	2,400	150	—
1.76	1,760	110	2400

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (80186 timer 0 & 80130 baud timer).

Timers

Input Frequencies

Reference: 2 MHz ± 0.1% (.5 μSec period nominal)
Event Rate: 2 MHz max.

80186 Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual (Cascaded) Timer/Counter	
	Min	Max	Min	Max
Real-time Interrupt	1.00 µs	65.535ms	6.00 µs	71.580 minutes
Programmable one-shot	1.50 µs	65.535ms	6.00 µs	71.580 minutes
Rate generator	2.342 Hz	1 MHz	.00023 Hz	333.333 KHz
Square-wave rate generator	2.342 Hz	1 MHz	.00023 Hz	333.333 KHz
Software triggered strobe	1.50 µs	65.535ms	6.50 µs	71.580 minutes
Event counter	—	2.00 MHz	—	—

Interfaces

Ethernet—IEEE 802.3 compatible
MULTIBUS®—IEEE 796 compatible
MULTIBUS®—Master D16 M24 I16 V0 EL

Compliance

iSBX™ Bus—IEEE P959 compatible
Serial I/O—RS-232C compatible, configurable as a data set or data terminal, RS-422A/RS-449

Connectors

Interface	Double-Sided Pins	Centers (in.)	Mating Connectors
Ethernet	10	0.1	AMP87531-5
MULTIBUS® SYSTEM	86 (P1)	0.156	Viking 3KH43/9AMK12 Wire Wrap
	60 (P2)	0.1	Viking 3KH30/9JNK
iSBX™ Bus 8-Bit Data	36	0.1	iSBX™ 960-5
16-Bit Data	44	0.1	iSBX™ 960-5
Serial I/O	26	0.1	3M 3452-0001 Flat or AMP88106-1 Flat

Physical Characteristics

Width—12.00 in. (30.48 cm)
Height—6.75 in. (17.15 cm)
Depth—0.70 in. (1.78 cm)
Weight—18.7 ounces

Environmental Characteristics

Operating Temperature—0°C to 55°C
Relative Humidity—10% to 90% (without condensation)

Electrical Characteristics

DC Power Supply Requirements

Configuration	Maximum Current (All Voltages ± 5%)		
	+5	+12	−12
SBC 186/51 as shipped:			
Board Total	6.70A	50mA	45mA
With separate battery back-up	5.90A	50mA	45mA
Battery back-up	.80A	—	—
With SBC-304 Memory Module Installed:			
Board Total	6.80A	50mA	45mA
With separate battery back-up	5.90A	50mA	45mA
Battery back-up	.90A	—	—

NOTES:
1. Add 150 mA to 5V current for each device installed in the 6 available Universal Memory Sites.
2. Add 500 mA to 12V current if Ethernet transceiver is connected.
3. Add additional currents for any SBX modules installed.

Reference Manual

122136-001—iSBC 186/51 Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 186/51	Communicating Computer